REMARKS

This responds to the Office Action mailed on April 9, 2008. Claims 1, 3, 6-20, 30, 33, 42, 50-54, 63 and 72-73 are amended, no claims are canceled, and no claims are added in this response. Claims 80-100 were previously canceled as being drawn to a non-elected group of claims. Thus, claims 1-79 remain pending in this application.

§*103 Rejection of the Claims*

Claims 1-79 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Horch et al. (U.S. Patent No. 6,965,129) in view of Baba (U.S. Patent No. 5,686,739) (*pages 2-54 of the Office Action*). Applicant respectfully traverses for at least the reasons that follow.

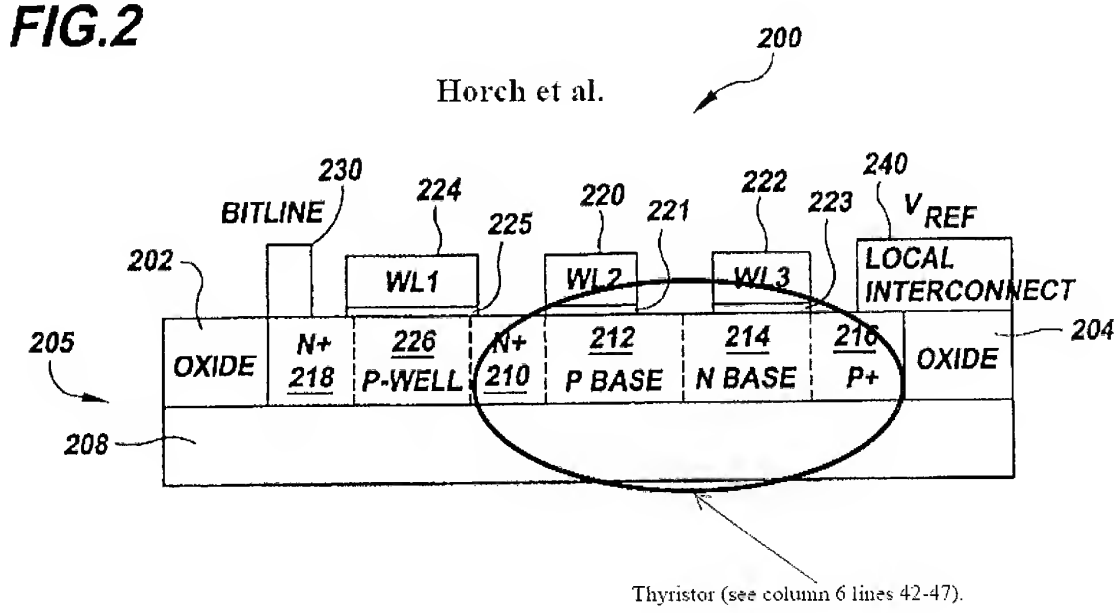
Claims 1-79 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nemati et al. (U.S. Patent No. 6,965,129) in view of Baba (U.S. Patent No. 5,686,739) (*pages 55-104 of the Office Action*). Applicant respectfully traverses for at least the reasons that follow.

Applicant notes that the Office Action is rather lengthy (104 pages). Rather than sequentially addressing every assertion contained therein, Applicant respectfully believes that a brief response will clarify the distinctions between the presently-pending claims and the references relied in the rejection. Applicant respectfully asserts that this response is sufficient to traverse the rejections.

The Office's position appears to be that it would be obvious to substitute the structure of Baba in place of the thyristor in the device of Horch et al. or in the device of Nemati et al.

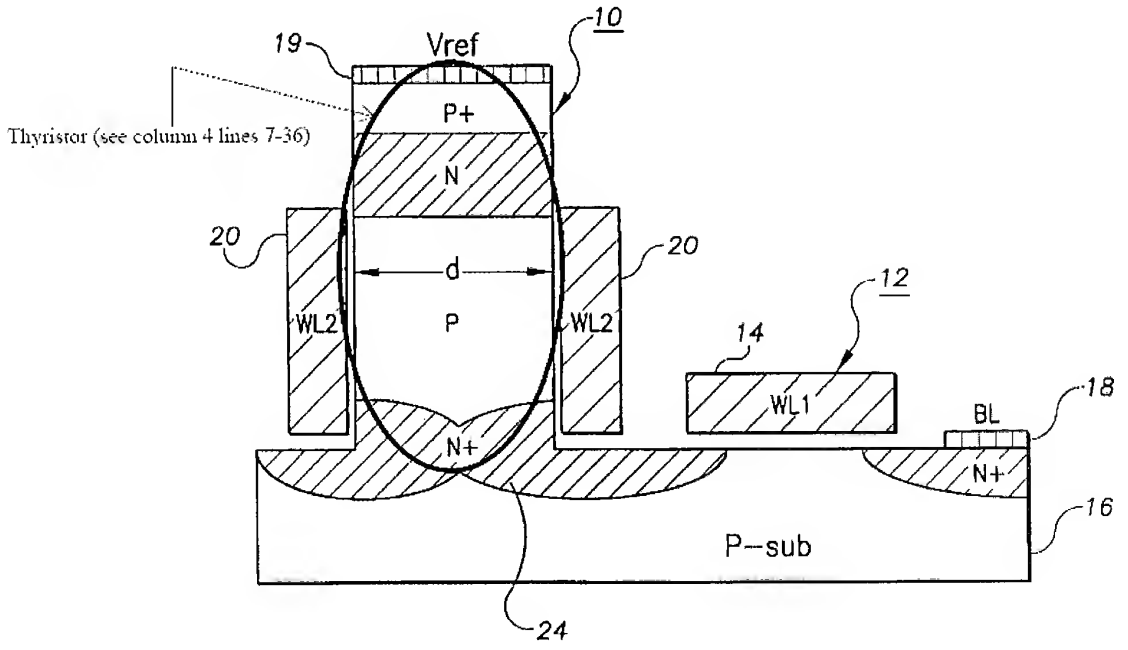
An example of the thyristor of Horch et al. is illustrated in FIG. 2.

FIG.2



An example of the thyristor of Nemati et al. is illustrated in FIG. 1.

FIG. 1 Nemati et al.



The Office appears to assert that the structure of either FIG. 1 or 2 in Baba is a PIN diode that could be substituted for the thyristor in either Horch et al. or Nemati et al. Applicant respectfully asserts that Baba neither shows nor suggests a PIN diode.

Rather, FIG. 1 of Baba is identified as prior art for Baba, and is further identified as a three terminal device that uses reverse-biased breakdown effects (col. 1 line 38 to col. 3 line 13). FIG. 1 is not a PIN diode. By way of example, region 11 is not an intrinsic region but rather is a doped region (col. 1 lines 40-42). Without an intrinsic region, the device of FIG. 1 cannot be a PIN diode.

Baba FIG. 1

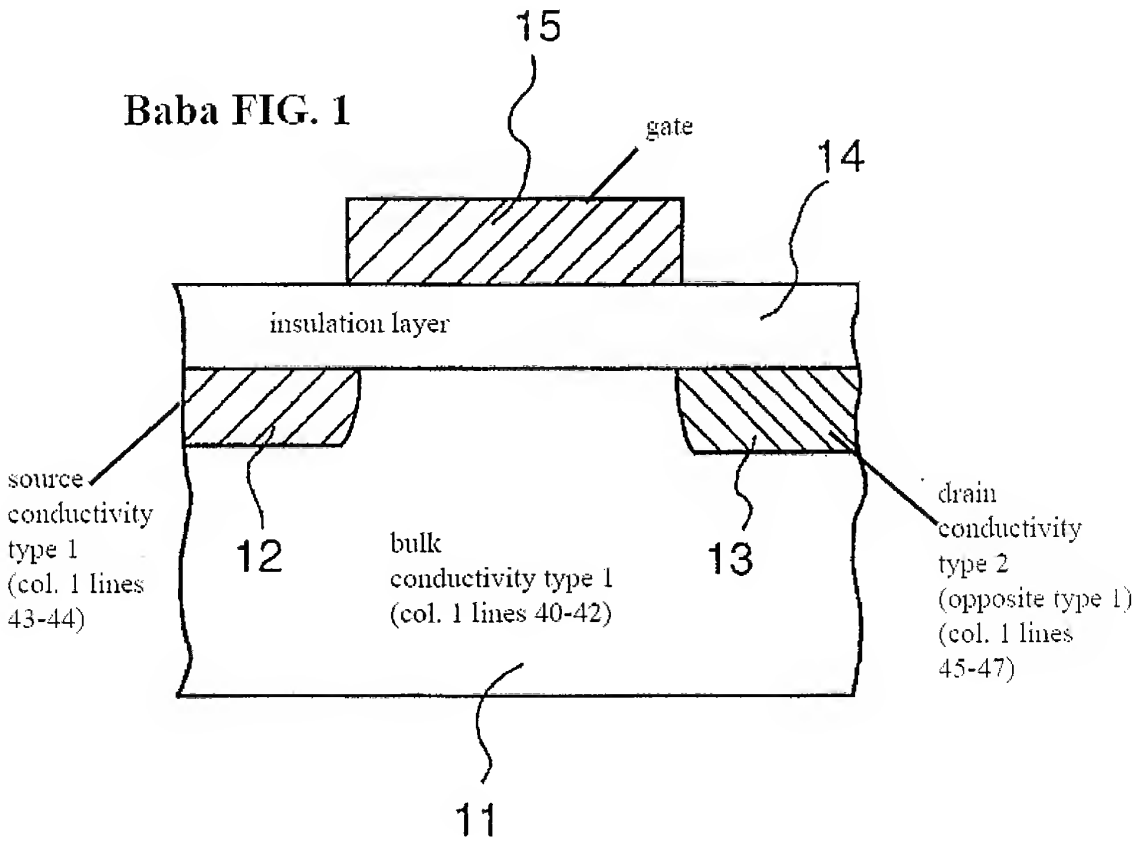
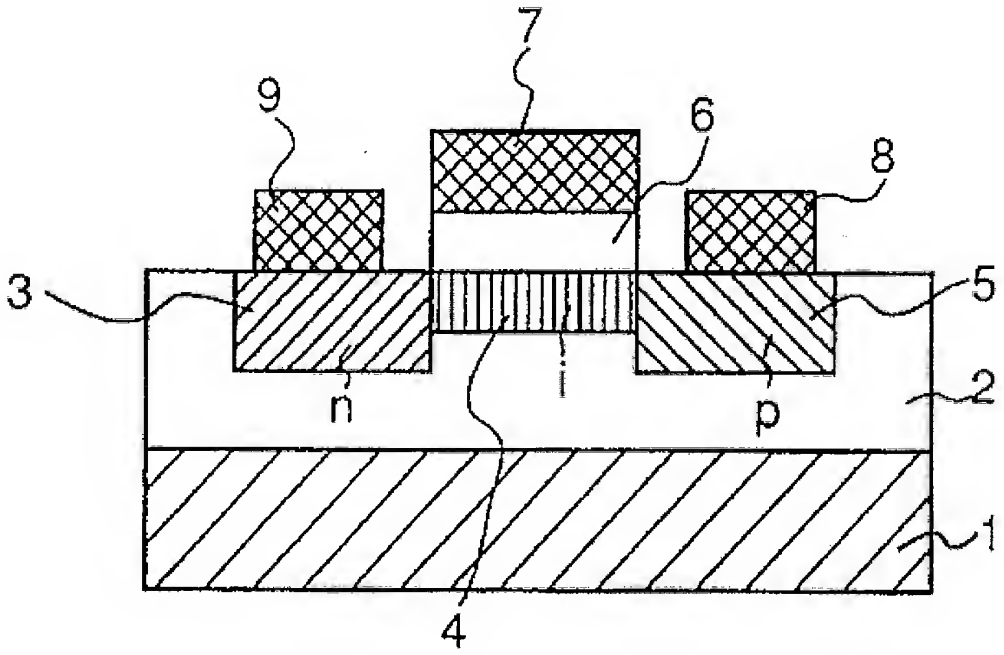
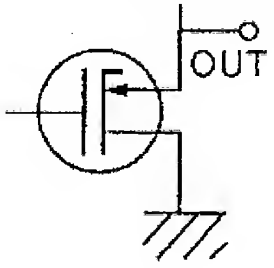


FIG. 2 of Baba is identified as a three terminal tunnel device.



This device is further illustrated in FIG. 3 as a field effect transistor.



Additionally, this device is claimed as a field effect transistor (see claims 1-26 of Baba). In an enhancement mode, a voltage needs to be applied to the gate before carriers will tunnel (col. 3 line 64 to col. 4 line 16), and the amount of tunneling current depends on the gate voltage magnitude (col. 4 lincs 17-22). No tunneling current will occur in the enhancement mode if no voltage or a low voltage is applied to the gate (control electrode) (col. 4 lines 30-36). In a depletion mode, a tunneling current will flow if no voltage is applied to the control electrode (col. 3 lines 37-45) and the tunneling current is interrupted if a predetermined voltage is applied to the control electrode (col. 3 lines 46-52). This describes the operation of a field effect tunneling transistor that requires the gate voltage signal to switch states.

In contrast, Applicant claims a diodc with an intrinsic region between the anode and cathode. A diode is different than a transistor. A diode gate is not necessary to switch states.

Some embodiments uses a diode gate to enhance switching. Applicant has chosen to further clarify the claims by clarifying that the diode is adapted to switch memory states without gating the diode (e.g. claim 1) and that embodiments where the diode is a gate-controlled diode (e.g. claim 3), the gating enhances the switching performance between memory states which already occurs without gating the diode. Further, Applicant respectfully asserts that the intrinsic region of Baba does not "assist with stabilizing the state of the memory cell".

Thus, Applicant respectfully asserts that neither the proposed combination of Horch et al. and Baba nor the proposed combination of Nemati et al. and Baba provide a diode with an intrinsic region between a cathode and anode, as recited in the claims.

Further, Applicant traverses the assertions and insinuations concerning the level of ordinary skill in semiconductor devices. For example, one of ordinary skill would not be well versed to solve all problems (e.g. thermodynamics and crystallography) in class 257. By way of analogy, one would expect an orthopedic surgeon to be adept at both knee surgery and brain surgery in spite of the fact that they are both surgical procedures performed by a doctor. Additionally, one of ordinary skill would not be a Nobel prize winner. Applicant acknowledges that one of ordinary skill will be educated, but traverses the characterization that the skill is "extremely" high. Further, Applicant traverses the insinuation that the Office knows that the "Court might easily have said that in the semiconductor art the person of ordinary skill is a person of extraordinary creativity." A person of ordinary skill in the art in semiconductor technology is also a person of ordinary creativity in the semiconductor technology.

Additionally, Applicant traverses the Office's insinuation that Horch et al. or Nemati et al. reasonably believed that various such as PMOS vs. NMOS access transistors, bulk vs. SOI substrates, NIP diodes, PIN diodes, vertical and lateral diodes are suggested to one of skill in the art by the explicit teachings, and thus did not describe these variations. Such a statement requires the Office to communicate with both Horch et al. and Nemati et al. in order to ascertain what they believed. Further, the assertion that "any objective observer" would believe that these variations are suggested is a conclusory statement that does not take into account the complexities of semiconductor design and fabrication, such as the need to accurately control the geometry of the intrinsic region to accurately and predictably control charge storage for the PIN diode. Conclusory statements are not sufficient to support the legal conclusion of obviousness.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6960 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 7-9-08

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Name

Signature